AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

1. (currently amended) A memory card conforming to a first operation standard, a second operation standard, and a third operation standard based on the first operation standard, comprising:

a non-volatile semiconductor memory having a plurality of semiconductor memory cells, wherein each said memory cell is capable of storing information, and

a controller that executes operation instructions to the non-volatile semiconductor memory based on received commands,

wherein[[:]] the controller controls a first data output timing that satisfies the first operation standard and the second operation standard, in a first operation mode, and controls a second data output timing that satisfies the third operation standard, in a second operation mode; and

wherein the controller includes a data timing switching unit that outputs data at a falling edge of a clock signal in the first data output timing, and outputs data at a rising edge of a clock signal in the second data output timing;

wherein the data timing switching unit includes:

a timing register to which one of the first data output timing and the second data output timing is set,

a first latch that latches an output data enable signal based on an inverted signal of the clock signal,

a second latch that latches the data based on the inverted signal of the clock signal,

a first selector that inputs the output data enable signal and a first latch signal outputted from the first latch, and selects and outputs one of the output data enable signal and the first latch signal based on a value set to the timing register, and

a second selector that inputs the data and a second latch signal outputted from the second latch, and selects and outputs one of the data and the second latch signal based on the value set to the timing register, and

wherein the data timing switching unit outputs:

the output data enable signal and the data to an output buffer from the first selector and the second selector, respectively, when the first data output timing is set to the timing register, and

the first latch signal and the second latch signal to the output buffer from the first selector and the second selector, respectively, when the second data output timing is set to the timing register,

wherein the output buffer outputs the data based on the output data enable signal to output the data at the rising edge of the clock signal, and outputs the data based on the second latch signal in synchronization with the first latch signal to output the data at the falling edge of the clock signal.

Claims 2-4. (cancelled)

5. (currently amended) A memory card conforming to a first operation standard, a second operation standard, and a

third operation standard based on the first operation standard, comprising:

a non-volatile semiconductor memory having a plurality of semiconductor memory cells, wherein each said memory cell is capable of storing information, and

a controller that executes operation instructions to the non-volatile semiconductor memory based on received commands,

wherein the controller controls a first data output timing that satisfies the first operation standard and the second operation standard, in a first operation mode, and controls a second data output timing that satisfies the third operation standard, in a second operation mode;

wherein the controller includes a timing delay switching unit that outputs data at a first delay time at the first data output timing, and outputs data at a second delay time being shorter than the first delay time at the second data output timing;

~~The memory card according to Claim 4,~~

wherein the timing delay switching unit includes:

a timing register to which one of the first data output timing and the second data output timing is set,

a first delay circuit that delays an output data enable signal by the first delay time,

a second delay circuit that delays the data by the first delay time,

a third delay circuit that delays the output data enable signal by the second delay time,

a fourth delay circuit that delays the data by the second delay time,

a third selector that inputs output data enable signals outputted from the first and second delay circuits,

and selects and outputs one of the two output data enable signals based on a value set to the timing register, and

a fourth selector that inputs respective data pieces outputted from the first and second delay circuits, and selects and outputs one of the data pieces based on the value set to the timing register, and

wherein the timing delay switching unit outputs:

the output data enable signal delayed by the first delay circuit and the data delayed by the second delay circuit to an output buffer from the third selector and the fourth selector, respectively, when the first data output timing is set to the timing register, and

the output data enable signal delayed by the first delay circuit and the data delayed by the fourth delay circuit to the output buffer from the third selector and the fourth selector, respectively, when the second data output timing is set to the timing register, and

wherein the output buffer outputs the data based on the output data enable signal.

Claims 6-7. (cancelled)

8. (currently amended) A memory card conforming to a first operation standard, a second operation standard, and a third operation standard based on the first operation standard, comprising:

a non-volatile semiconductor memory having a plurality of semiconductor memory cells, wherein each said memory cell is capable of storing information; and

a controller that executes operation instructions to the non-volatile semiconductor memory based on received commands;

wherein the controller controls a first data output timing that satisfies the first operation standard and the second operation standard, in a first operation mode, and controls a second data output timing that satisfies the third operation standard, in a second operation mode;

~~The memory card according to Claim 6,~~

wherein the controller includes a data output time adjustment unit that adjusts a rise time/fall time of the data in the first data output timing, so that the rise time/fall time of the data is faster for the second data output timing than for the first data output timing; and

wherein the data output time adjustment unit includes:

a timing register to which one of the first data output timing and the second data output timing is set,

an output buffer that outputs data based on an output data enable signal, when one of the first data output timing and the second data output timing is set to the timing register,

a plurality of auxiliary output buffers that output data based on the output data enable signal at the second data output timing, and

an auxiliary output buffer enable unit that outputs the output data enable signal to one of the auxiliary output buffers in correspondence with a power consumption parameter set to a power consumption parameter register, when the second data output timing is set to the timing register.

9. (currently amended) A memory card conforming to a first operation standard, a second operation standard, and a third operation standard based on the first operation standard, comprising:

a non-volatile semiconductor memory having a plurality of semiconductor memory cells, wherein each said memory cell is capable of storing information, and

a controller that executes operation instructions to the non-volatile semiconductor memory based on received commands,

wherein the controller controls a first data output timing that satisfies the first operation standard and the second operation standard, in a first operation mode, and controls a second data output timing that satisfies the third operation standard, in a second operation mode;

wherein the controller includes a timing delay switching unit that outputs data at a first delay time at the first data output timing, and outputs data at a second delay time being shorter than the first delay time at the second data output timing;

~~The memory card according to Claim 1,~~

wherein the controller includes:

the power consumption parameter register to which are set power consumption parameters that specify respective power consumptions,

a clock generator that generates a clock signal,

a plurality of frequency dividers that output to divide a frequency of the clock signal generated by the clock generator into different frequencies, and

a system clock selector that selects one of a plurality of clock signals outputted from the plurality of frequency dividers based on a power consumption parameter set to the power consumption parameter register, and that supplies the selected clock signal as a system clock, and

wherein the system clock selector selects the system clock of a higher frequency, as the power consumption

parameter becomes a value larger than a default value corresponding to a minimum power consumption.

10. (previously presented) The memory card according to Claim 1, including a plurality of non-volatile semiconductor memories, wherein the controller controls a number of said non-volatile semiconductor memories in parallel operation, said number depending upon the power consumption parameter set to the power consumption parameter register.

Claims 11-14. (cancelled)

15. (new) The memory card according to Claim 5, including a plurality of non-volatile semiconductor memories, wherein the controller controls a number of said non-volatile semiconductor memories in parallel operation, said number depending upon the power consumption parameter set to the power consumption parameter register.

16. (new) The memory card according to Claim 8, including a plurality of non-volatile semiconductor memories, wherein the controller controls a number of said non-volatile semiconductor memories in parallel operation, said number depending upon the power consumption parameter set to the power consumption parameter register.

17. (new) The memory card according to Claim 9, including a plurality of non-volatile semiconductor memories, wherein the controller controls a number of said non-volatile semiconductor memories in parallel operation, said number

depending upon the power consumption parameter set to the power consumption parameter register.